We claim:

1. A method of combined modulation and Forward Error Correction (FEC) coding of data bit signals for transmission over a communications channel comprising:

FEC coding a subset of the data bit signals using an LDPC code to produce FEC coded bit signals;

modulating the data bit signals and the FEC coded bit signals using at least one constellation that contains more than one bit signal; and

designating a coset of the at least one constellation using the FEC coded bit signals.

2. The method of claim 1, wherein the modulation is single-carrier or multicarrier modulation.

3. The method of claim 1, wherein the LDPC code has an equal BER for one or more information bits and one or more parity bits.

4. The method of claim 1, wherein an LDPC code parity check matrix is determined during an initialization or a configuration phase.

5. The method of claim 1, wherein an LDPC code generator matrix is determined during an initialization or a configuration phase.

6. The method of claim 1, wherein a LDPC code parity check matrix is determined after a latency and a data rate are specified.

7. The method of claim 1, wherein a LDPC code generator matrix is determined after a latency and a data rate are specified.

8. The method of claim 1, wherein the LDPC code has a variable codeword length.

9. The method of claim 8, wherein the codeword length is varied depending on one or more of a data rate and a latency.

10. The method of claim 1, wherein the LDPC code does not have any cycles.

11. The method of claim 1, wherein a parity check matrix of the LDPC code has an equal number of branches connecting at least one information bit and at least one parity bit with at least one parity node.

12. The method of claim 1, wherein a parity check matrix contains at least one parity node connected to an equal number of information bits and parity bits.

13. A method of forward error correction coding of data bit signals using LDPC codes comprising:

determining at least one of a data rate and a latency; and

determining a LDPC generator matrix that encodes data bit signals.

14. The method of claim 13, wherein the at least one of a data rate and a latency are determined during an initialization or a configuration phase.

15. The method of claim 13, wherein the LDPC generator matrix is determined after the data rate and the latency have been determined.

16. The method of claim 13, wherein the LDPC code has a variable codeword length.

17. The method of claim 16, wherein the codeword length is varied depending on one or more of the data rate and the latency.

18. The method of claim 13, wherein the LDPC code does not have any cycles.

19. A method of forward error correction decoding of data bit signals using LDPC codes comprising:

determining at least one of a data rate and a latency; and

determining a LDPC parity check matrix that decodes coded bit signals.

20. The method of claim 19, wherein the at least one of a data rate and a latency are determined during an initialization or a configuration phase.

21. The method of claim 19, wherein the LDPC parity check matrix is determined after the data rate and the latency have been determined.

22. The method of claim 19, wherein the LDPC code has a variable codeword length.

23. The method of claim 22, wherein the codeword length is varied depending on one or more of the data rate and the latency.

24. The method of claim 19, wherein the LDPC code does not have any cycles.

25. An information storage media comprising information that performs forward error correction coding of data bit signals using LDPC codes comprising:

information that determines at least one of a data rate and a latency; and

information that determines a LDPC generator matrix that encodes data bit signals.

26. The media of claim 25, wherein the at least one of a data rate and a latency are determined during an initialization or a configuration phase.

27. The media of claim 25, wherein the LDPC generator matrix is determined after the data rate and the latency have been determined.

28. The media of claim 25, wherein the LDPC code has a variable codeword length.

29. The media of claim 28, wherein the codeword length is varied depending on one or more of the data rate and the latency.

30. The media of claim 25, wherein the LDPC code does not have any cycles.

31. An information storage media comprising information that performs forward error correction decoding of data bit signals using LDPC codes comprising:

information that determines at least one of a data rate and a latency; and

information that determines a LDPC parity check matrix that decodes the coded bit signals.

32. The media of claim 31, wherein the at least one of a data rate and a latency are determined during an initialization or a configuration phase.

33. The media of claim 31, wherein the LDPC parity check matrix is determined after the data rate and the latency have been determined.

34. The media of claim 31, wherein the LDPC code has a variable codeword length.

35. The media of claim 34, wherein the codeword length is varied depending on one or more of a data rate and a latency requirement.

36. The media of claim 31, wherein the LDPC code does not have any cycles.